

P-CHANNEL DIFFUSED SILICON TETRODE FIELD-EFFECT TRANSISTOR

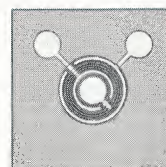
TYPE 3N89

DUAL-GATE UNIFET

- Separate signal and control gates
- Low gate number 1 input and transfer capacitances
- High g_{fs}/I_{DSS} and g_{fs}/C_{giss}
- Gate number 2 control of g_{fs} , V_P , and I_{DSS}

FOR:

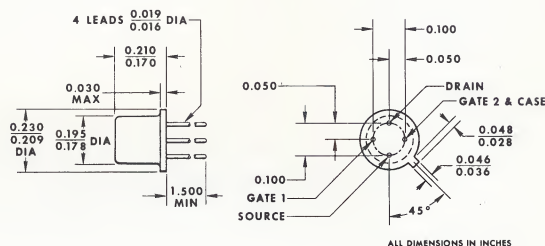
H-F amplifiers
AGC amplifiers
Mixers
Choppers
High-gain micropower amplifiers



20 mils square

*MECHANICAL DATA 4-lead TO-18 Package

Gate number 2 is in electrical contact with the case.



PRODUCT CONDITIONING

Each unit receives the following treatment before final electrical test:

High Temperature Storage: 72 hours at 150°C
Thermal Shock: +200 to -65°C for 5 cycles
35,000g Centrifuge in the Y₁ Plane
Helium and Gross Leak Tests for Hermeticity
Impressed Voltage Burn-In: 24 hours at 150°C with $V_{G1S} = V_{G2S} = 24$ v, $V_{DS} = 0$
Post-Bake Clean-Up to Assure Solderability

*ABSOLUTE MAXIMUM RATINGS AT 25°C

Gate-Drain Voltage	30 v
Gate 1 Current	10 ma
Gate 2 Current	30 ma
Drain Current	50 ma
Continuous Device Dissipation at 25°C free air temp. Derate 2 mw/°C	300 mw
Storage Temperature	-65 to +150°C
Lead Temperature at 1/16" from case for 10 sec	255°C

*JEDEC Registered Data

Siliconix incorporated

**ELECTRICAL CHARACTERISTICS AT 25°C except as noted
Gate 1 shorted to Gate 2**

Characteristic	Test Conditions	Min	Typ	Max	Unit
*I _{GSS}	Gate-Source Cutoff Current $V_{G1S} = V_{G2S} = 20 \text{ v}$ $V_{DS} = 0$			5	na
*I _{GSS}	Gate-Source Cutoff Current $V_{G1S} = V_{G2S} = 20 \text{ v}$, $T_A = 150^\circ\text{C}$ $V_{DS} = 0$			5	μa
*BV _{GDS}	Gate-Drain Breakdown Voltage $I_G = 1 \mu\text{a}$ $V_{DS} = 0$ $V_{G1G2} = 0$	30			v
*I _{DSS}	Drain Current at Zero Gate Voltage $V_{DS} = -5 \text{ v}$ $V_{G1S} = V_{G2S} = 0$	-0.5	-1.2	-2.5	ma
*V _P	Gate-Source Pinch-Off Voltage $V_{DS} = -5 \text{ v}$ $I_D = -1 \mu\text{a}$ $V_{G1G2} = 0$	1	2	4	v
g_{fs}	Small-Signal Common-Source Forward Transconductance $V_{DS} = -5 \text{ v}$ $V_{G1S} = V_{G2S} = 0$		1200		μmho

**ELECTRICAL CHARACTERISTICS AT 25°C
Gate 1 isolated from Gate 2**

Characteristic	Test Conditions	Min	Typ	Max	Unit
V _{P1}	Gate 1-Source Pinch-Off Voltage (Note 1) $V_{DS} = -5 \text{ v}$ $I_D = -1 \mu\text{a}$ $V_{G2S} = 0$		3.3		v
V _{P2}	Gate 2-Source Pinch-Off Voltage (Note 2) $V_{DS} = -5 \text{ v}$ $I_D = -1 \mu\text{a}$ $V_{G1S} = 0$		10		v
*I _{G1}	Gate 1-Current (Note 3) $V_{DG1} = -5 \text{ v}$ $V_{G2S} = 0$ $I_D = -250 \mu\text{a}$			0.6	na
*I _D	Drain Current at Gate-Gate Reach Through (Note 4) $V_{DS} = -5 \text{ v}$ $I_{G1} = 1 \text{ na}$ $V_{G2S} = 0$			-100	μa
*I _D	Drain Current at Gate-Gate Reach Through (Note 5) $V_{DS} = -5 \text{ v}$ $I_{G1} = -1 \text{ na}$ $V_{G1S} = 0$			-100	μa
* g_{fs1}	Small-Signal Common-Source Gate 1 Forward Transconductance (Note 6) $V_{DS} = -5 \text{ v}$ $V_{G2S} = 0$ $V_{G1S} = 0$ $V_{G2S} = 0$ $f = 1 \text{ kc}$	450	800	1300	μmho
g_{fs2}	Small-Signal Common-Source Gate 2 Forward Transconductance (Note 7) $V_{DS} = -5 \text{ v}$ $V_{G1S} = 0$ $V_{G2S} = 0$ $V_{G1S} = 0$ $f = 1 \text{ kc}$		400		μmho
*C _{g1ss}	Gate 1-Source Capacitance (Note 8) $V_{DS} = -5 \text{ v}$ $V_{G2S} = 0$ $V_{G1S} = 1 \text{ v}$ $f = 1 \text{ kc}$		2.5	3.0	pf
C _{g2ss}	Gate 2-Source Capacitance (Note 9) $V_{DS} = -5 \text{ v}$ $V_{G1S} = 0$ $V_{G2S} = 1 \text{ v}$ $f = 1 \text{ kc}$		5.7		pf
*C _{dg1}	Gate 1-Drain Capacitance $V_{DS} = -5 \text{ v}$ $V_{G2S} = 0$ $V_{G1S} = 1 \text{ v}$ $f = 1 \text{ kc}$		0.6	0.9	pf
C _{dg2}	Gate 2-Drain Capacitance (Note 8) $V_{DS} = -5 \text{ v}$ $V_{G1S} = 0$ $V_{G2S} = 1 \text{ v}$ $f = 1 \text{ kc}$		1.8		pf

*JEDEC Registered Data

NOTES:

1. V_{P1} measured with gate 2 shorted to source
2. V_{P2} measured with gate 1 shorted to source
3. Gate 1 current under operating conditions below break point of V_{G1S} vs I_{G1} input characteristics. See graph and Note, page 3
4. Maximum drain current under gate-gate reach through due to impressed V_{G1S}
5. Maximum drain current under gate-gate reach through due to impressed V_{G2S}
6. Signal applied to gate 1 only
7. Signal applied to gate 2 only
8. Includes approximately 1 pf header capacitance
9. Includes approximately 3 pf header capacitance

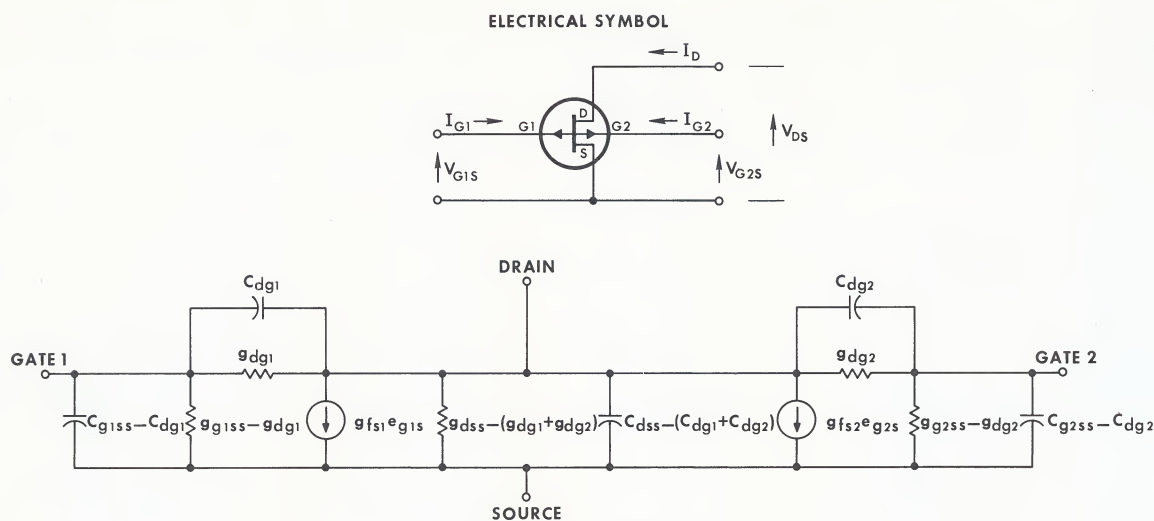


Fig. 1 Equivalent Circuit

Dual-gate construction provides unique control characteristics which are presented in Figs. 4-6 for a typical device. The effective I_{DSS} , V_P , and g_{fs} may be modified as desired by application of a control voltage from gate 2 to source. The controlling effect is apparent in the parametric curves of Fig. 4; specific values referenced to $V_{G2S} = 0$ conditions are presented vs V_{G2S} in Fig. 5. The dual-gate UNIFET is particularly useful in micropower amplifiers due to a high value of g_{fs}/I_D at increased V_{G2S} as is shown in Fig. 6. As V_{G2S} is increased, g_{fs}/I_D will eventually peak and decrease rapidly as g_{fs} approaches zero. The useful range in this application is limited to $V_{G2S} = 8.5$ v for a typical unit.

Because the dual-gate construction permits separation of control and signal functions with an attendant reduction in gate 1 associated capacitances, the dual-gate UNIFET has specific applicability for use in HF and/or AGC amplifiers. A typical device in the circuit of Fig. 7 provides ≈ 20 db power gain at 45 mc and an AGC range of >30 db without detuning.

TYPICAL DC CHARACTERISTICS

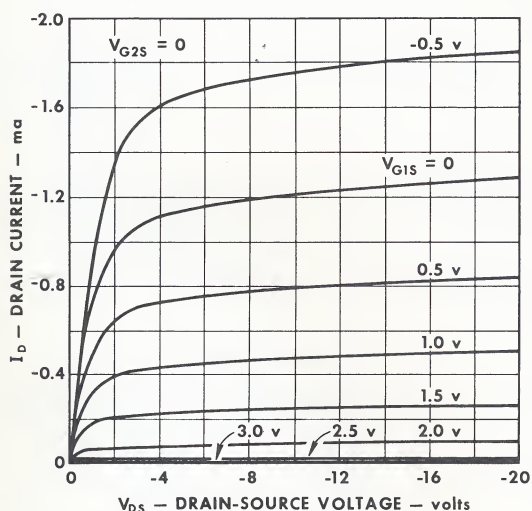


Fig. 2 Output Characteristics

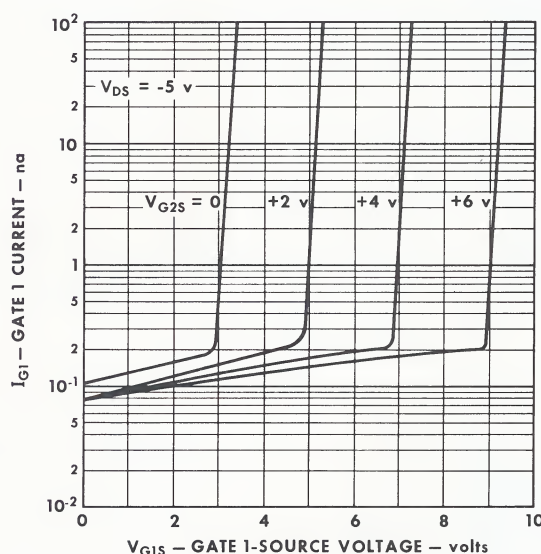


Fig. 3 Input Characteristics

Note:

Careful notice should be taken of the discontinuities of input characteristics shown in Fig. 3. The break points are due to gate-to-gate reach-through current. As the break occurs slightly below V_{P1} it will be undesirable to operate near V_{P1} in most applications when $V_{G2S} = 0$.

GATE 2 CONTROL FUNCTIONS — TYPICAL CHARACTERISTICS

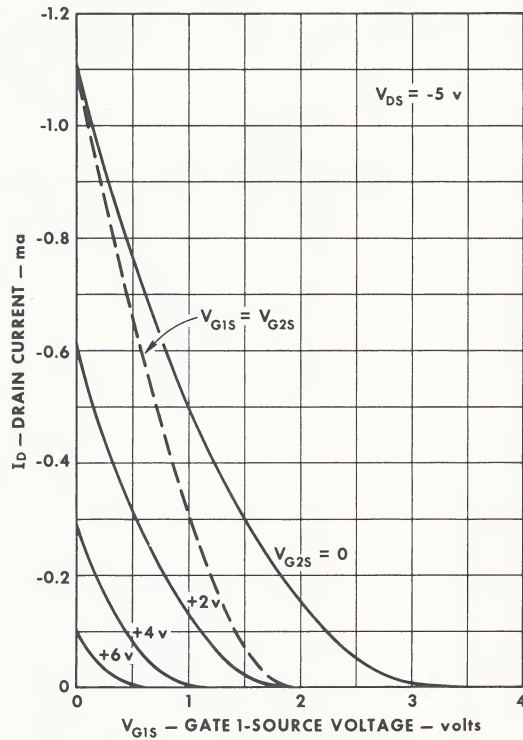
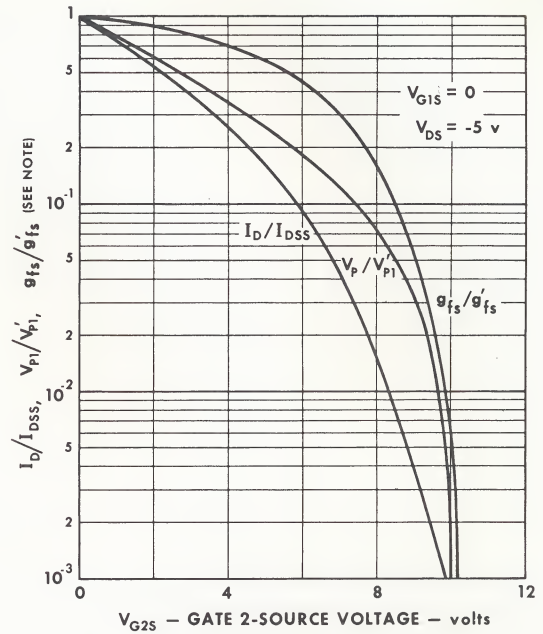


Fig. 4 Transfer Characteristics



Note:

I_{DSS} and g'_{fs} are the specific values of I_D and g'_{fs} when $V_{G1S} = V_{G2S} = 0$
 V'_{P1} is specific value of V_{P1} when $V_{G2S} = 0$

Fig. 5 Control Effect of Gate 2

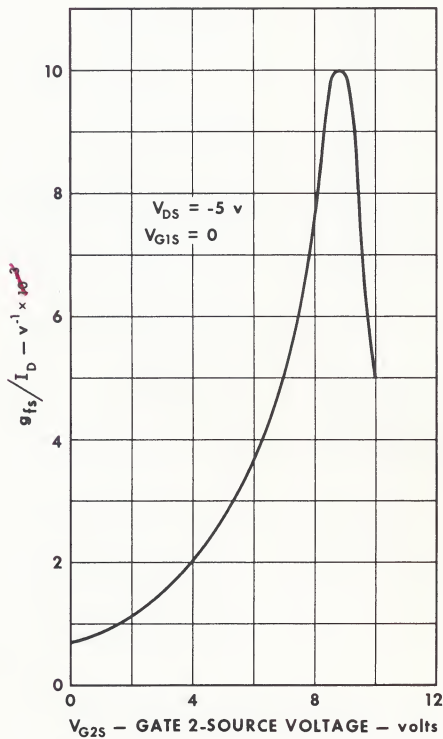


Fig. 6 g'_{fs}/I_D vs V_{G2S}

CIRCUIT APPLICATION

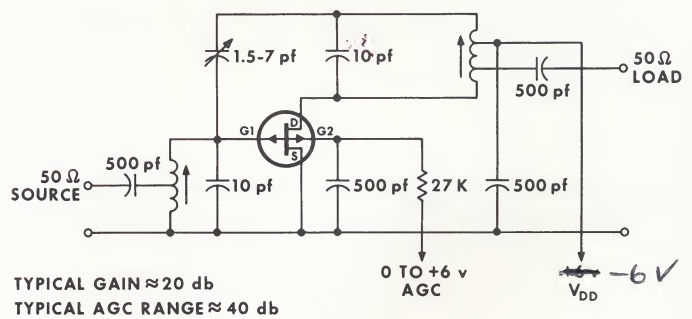


Fig. 7 45-mc Amplifier

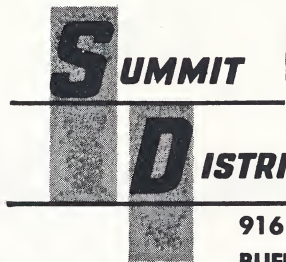
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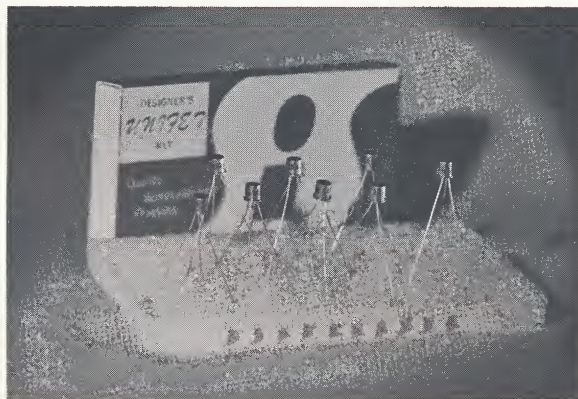
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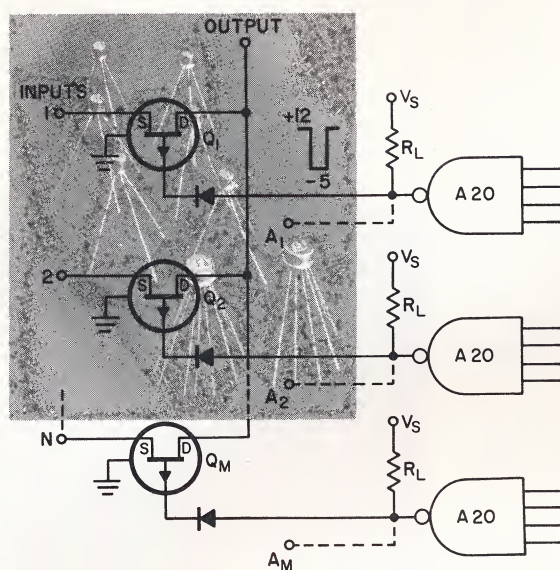
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